

WHAT IS CLAIMED IS:

1 1. A method of forming a fin-shaped channel region, the method
2 comprising:

3 providing a compound semiconductor layer above an insulating layer;
4 providing a trench in the compound semiconductor layer;

5 providing a strained semiconductor layer above the compound
6 semiconductor layer and within the trench, the trench being associated with
7 the fin-shaped channel region;

8 removing the strained semiconductor layer from above the compound
9 semiconductor layer, thereby leaving the strained semiconductor layer within
10 the trench; and

11 removing the compound semiconductor layer to leave the strained
12 semiconductor layer and form the fin-shaped channel region.

1 2. The method of claim 1, further comprising providing an oxide
2 material adjacent lateral sidewalls of the fin shaped channel region.

1 3. The method of claim 2, further comprising:

2 providing a gate conductor over the oxide material.

1 4. The method of claim 1, wherein the fin-shaped channel region
2 includes silicon (Si).

1 5. The method of claim 4, wherein compound semiconductor layer
2 is a silicon germanium layer.

1 6. The method of claim 4, wherein the first removing step is a
2 polishing step.

1 7. The method of claim 6, wherein the second removing step is an
2 etching step selective to silicon germanium.

1 8. The method of claim 1, wherein the second removing step
2 utilizes a mask, the mask protecting portions of the compound
3 semiconductor layer for a source region and a drain region.

1 9. The method of claim 1, wherein the fin-shaped channel region
2 has an aspect ratio of between approximately 4 and 6.

1 10. A method of FinFET channel structure formation, the method
2 comprising:
3 providing a first layer above an insulating layer above a substrate, the
4 first layer including silicon and germanium;
5 providing an aperture in the first layer, the aperture extending to the
6 insulating layer;
7 providing a strained material within the aperture; and
8 removing the first layer to leave the strained material.

1 11. The method of claim 10, wherein the removing step is an
2 etching step selective to silicon germanium.

1 12. The method of claim 10, wherein the strained material is
2 provided by selective silicon epitaxy.

1 13. The method of claim 10, further comprising forming a gate
2 dielectric structure along sidewalls and a top of the strained material.

1 14. The method of claim 13, wherein the strained material is
2 provided above the first layer.

1 15. The method of claim 14, wherein strained material is removed
2 from above the first layer by a chemical mechanical polish step.

1 16. The method of claim 15, wherein the first layer is protected by
2 a mask during the removing step at a source location and a drain location.

1 17. A method of fabricating an integrated circuit including a fin-
2 based transistor, the method comprising steps of:

3 providing an insulative material;

4 providing a strain inducing layer above the insulative material;

5 providing an aperture in the strain inducing layer;

6 forming a strained material in the aperture by selective epitaxial
7 growth;

8 removing at least a portion of the strain inducing layer to thereby leave
9 the strained material as a fin structure; and

10 providing a gate structure for the fin structure.

1 18. The method of claim 17, wherein the aperture is between
2 approximately 20 and 120nm wide.

1 19. The method of claim 17, wherein the removing step is a dry
2 etching step selective to silicon germanium with respect to silicon.

3 20. The method of claim 17, wherein the gate structure includes
4 polysilicon.